Electronic Version
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Claims

[c1] 1.A self-timed data transmission system, comprising:
a data bit group defined by at least two data bits to be transmitted from a corresponding plurality of transmitting storage elements;
a corresponding plurality of data receiving storage elements for receiving the data transmitted from said transmitting storage elements;
encoding logic for encoding the transmitted data from said transmitting storage elements, wherein said encoded transmitted data is coupled to a plurality of data lines; and
wherein said encoding logic is further configured so as to result in only one of said plurality of data lines being activated during a given data transmission cycle.

[c2] 2.The system of claim 1, wherein said plurality of data lines further comprises a true line and a complementary line for each data bit within said data bit group.

[c3] 3.The system of claim 2, wherein said data bit group comprises two data bits.

[c4] 4.The system of claim 1, further comprising decoding

logic for decoding the encoded transmitted data on said plurality of data lines, said decoding logic coupled to said data receiving storage elements.

[c5] 5.The system of claim 1, wherein said plurality of data lines are precharged prior to a data transmission operation and said activating only one of said plurality of data lines a given data transmission cycle comprises discharging said only one of said plurality of data lines.

[c6] 6.A self-timed, digital data input/output (I/O) path transmission system, comprising:
a data bit group defined by at least two data bits to be transmitted from a corresponding plurality of transmitting latches;
a corresponding plurality of data receiving storage latches for receiving the data transmitted from said transmitting latches;
encoding logic for encoding the transmitted data from said transmitting latches, wherein said encoded transmitted data is coupled to a plurality of data lines;
decoding logic for decoding the encoded transmitted data on said plurality of data lines, said decoding logic coupled to said receiving latches;
wherein said encoding logic is further configured so as to result in only one of said plurality of data lines being activated during a given data transmission cycle.

[c7] 7.The system of claim 6, wherein said plurality of data lines further comprises a true line and a complementary line for each data bit within said data bit group.

[c8] 8.The system of claim 7, wherein said data bit group comprises two data bits.

[c9] 9.The system of claim 6, wherein said receiving latches further comprise set/reset (S-R) latches.

[c10] 10.The system of claim 9, wherein a logic 0 data bit is stored in a given receiving latch upon discharge of a set node associated therewith, and wherein a logic 1 data bit is stored in said given receiving latch upon discharge of a reset node associated therewith.

[c11] 11.The system of claim 6, wherein said plurality of data lines are precharged prior to a data transmission operation and said activating only one of said plurality of data lines a given data transmission cycle comprises discharging said only one of said plurality of data lines.

[c12] 12.The system of claim 11, wherein said encoding logic comprises a plurality of NAND gates, each of said NAND gates having one of a true/complement node from a first transmission latch as a first input thereto, and one of a true/complement node from a second transmission latch

as a second input thereto.

[c13] 13.The system of claim 12, wherein said only one of said plurality of data lines discharged during a given clock cycle corresponds to the data line coupled to the one of said NAND gates having logic 1 as first and second inputs thereto.

[c14] 14.A method for transmitting self-timed data within a multiple input/output (I/O) data path, the method comprising:
configuring the data path into data bit groups defined by at least two data bits to be transmitted from a corresponding plurality of transmitting storage elements;
encoding the data from said transmitting storage elements and coupling said encoded onto a plurality of data lines; and
decoding the data from said plurality of data lines, said decoded data thereafter received by a corresponding plurality of data receiving storage elements;
wherein said encoding the data is implemented in a manner so as to result in only one of said plurality of data lines being activated during a given data transmission cycle.

[c15] 15.The method of claim 14, wherein said plurality of data lines further comprises a true line and a comple-

mentary line for each data bit within said data bit group.

[c16] 16.The method of claim 15, wherein said data bit group comprises two data bits.

[c17] 17.The method of claim 14, further comprising precharging said plurality of data lines prior to a data transmission operation and wherein said activating only one of said plurality of data lines a given data transmission cycle comprises discharging said only one of said plurality of data lines.